A GaAs MONOLITHIC 6—18 GHz MEDIUM POWER AMPLIFIER

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ABSTRACT

A monolithic two-stage medium power amplifier, fabricated on GaAs and designed to cover the 6-18 GHz frequency band, is described. Amplifier circuit topology, process sequence, and measured performance results are presented. Chips from several epitaxial and ion implanted slices have demonstrated good output power and gain performance across the 7.0-17.0 GHz band, achieving an average of 27.3 dBm (540 mW or 0.45 watts per millimeter of gate width) at 18.8 percent power-added efficiency, with an average gain of 10.6 dB, at 1 dB gain compression.

INTRODUCTION

The success of a new generation of electronic warfare systems requires the development of high performance solid-state microwave power amplifiers suited for volume production at low cost. GaAs monolithic microwave integrated circuit (MMIC) technology offers the potential of meeting this challenge. This paper addresses the design and initial performance results of a broad bandwidth, medium power MMIC amplifier intended for EW application. Performance goals for the amplifier design are shown in Table I.

TABLE I. MONOLITHIC MEDIUM POWER AMPLIFIER PERFORMANCE GOALS

Frequency Range	6.0 - 18.0 GHz
Small-signal Gain	7.0 dB, minimum
Gain Ripple	2.0 dB, maximum
Output Power at 1 dB Gain Compression (CW)	400 mW, minimum
Power-added Efficiency at 1 dB Gain Compression	20% minimum

DESIGN APPROACH

A single-ended, bandpass, two-FET cascade was chosen as the basic circuit topology for the monolithic medium power amplifier. A symmetrical circuit topology was selected to give the option of applying bias supply voltages from either side of the chip. Incorporation of integral bias networks necessitates the bandpass matching network approach. The two-stage single-ended cascade represents a compromise between maximizing the gain per monolithic chip and obtaining a reasonable quantity of functional chips per slice, based on current GaAs processing yields.

A 900-micron gate width FET was used for the input device and two 600-micron FETs in parallel, for a total of 1200-micron, were used for the output device. The "split" 1200-micron device was chosen to decrease source inductance and to diffuse heat concentration in the device. A 0.10-millimeter GaAs substrate thickness was selected for these same reasons.

Computer-aided-design (CAD) programs were used extensively throughout the design of the 900-1200 micron monolithic amplifier. SUPER-COMPACT was used for the analysis and optimization of the various circuit elements. An in-house program was utilized to predict power performance and, in conjunction with SUPER-COMPACT, to design matching circuits for maximum amplifier output power.

Models for the 900-micron and 600-micron FETs were derived from data obtained from discrete GaAs FETs and previously built GaAs FET hybrid power amplifiers. The various FET model parameters were optimized using CAD techniques to match the measured data.

The design of the matching circuits progressed from amplifier output to input. After the initial optimization of the matching network was complete, microstrip discontinuities were added, and a final optimization was performed. Due to the constraints placed on the amplifier in the initial planning stages, each network layout was completed following its design. This ensured that the network was realizable, while meeting the performance goals of the amplifier; if not, the network design was re-iterated. Finally, an analysis was performed to determine the sensitivity of the amplifier performance to fabrication tolerances. If an element was found to be too sensitive, adjustments were made, and the network was re-optimized.

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Achieving a producible monolithic circuit design requires an understanding of the performance sensitivities to process variations. Extensive sensitivity analyses, involving Monte Carlo statistical techniques, provide insight into the expected performance distribution in volume production and the critical RF yield drivers. Sensitivity analyses were a major component of the 900-1200 micron amplifier design process.

Figure 1 shows the circuit schematic of the 900-1200 micron amplifier. A photograph of the chip is shown in Figure 2, and the predicted gain and power responses are presented in Figure 3.

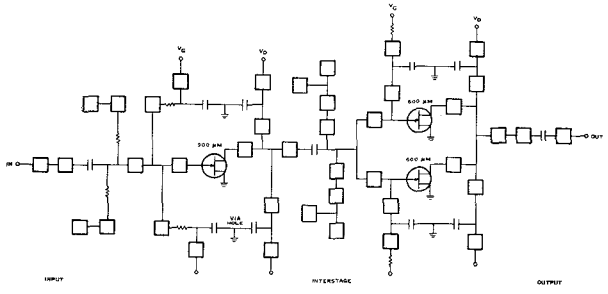

Figure 1. 900-1200 Micron Amplifier Circuit Schematic

MMIC PROCESSING

The 900-1200 micron amplifier was fabricated using both epitaxial and ion implanted material, with comparable performance results. In both cases, two-inch LEC substrates were used as the starting material. For epitaxial work, the substrates are etched and the $AsCl_3$ process is used to grow the buffer and active layers. The active layer is doped to approximately 1.5-1.8E17 in both types of material.

The first step in the process sequence is patterning and etching the active layer for device isolation. Next, the source-drain metallization and resistors are formed using alloyed AuGeNi, with a resistivity of approximately 1.9 ohms per square. All levels except gate definition are formed using optical contact photolithography, usually with the well known chlorobenzene technique to enhance liftoff. The recessed TiPtAu gates are defined using E-beam lithography, yielding a 0.5-micron gate length.

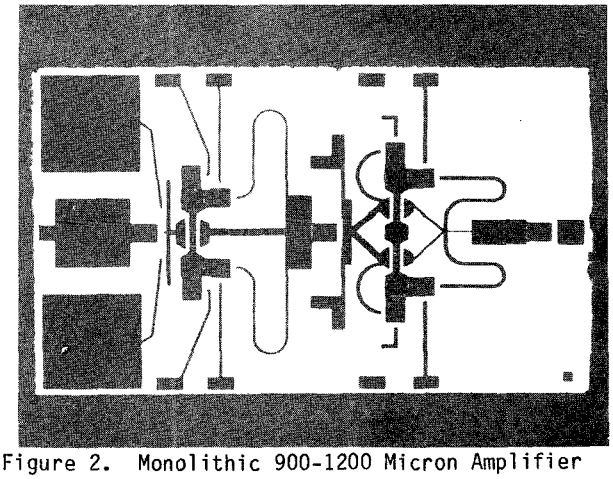

Figure 2. Monolithic 900-1200 Micron Amplifier

First level metallization forms the transmission lines and overlays the device "bond pads," increasing the conductivity over the AuGeNi. A 0.4-micron plasma-deposited layer of silicon nitride forms the capacitor dielectric and provides passivation. Fabrication of the top capacitor plates follows the nitride deposition.

The air-bridge/plating sequence consists of the following steps. Resist is applied and patterned, and the exposed nitride etched away. Then, a thin layer of gold is sputtered onto the slice, and another layer of resist is applied and patterned with the air-bridge mask. The transmission lines, bonding pads, capacitor top plates, as well as the air-bridges, are plated.

The slice is lapped to 0.1-millimeter and via holes are formed using reactive-ion-etching. The backside is metallized and plated, and the slice is sawed into separate bars.

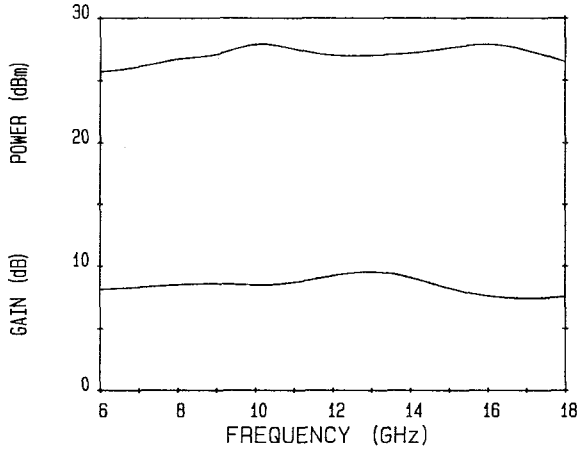

Figure 3. Predicted Amplifier Performance at 1 dB Gain Compression

PERFORMANCE RESULTS

The first design iteration achieved the performance results described in this section. No tuning was performed either on the MMIC or the test fixture. Figure 4 shows measured gain and output power at 1 dB gain compression obtained from typical 900-1200 micron medium power amplifiers fabricated on epitaxial and ion implanted substrates. Measured amplifier bandwidth is less than predicted, covering the 7.0-17.0 GHz frequency band, with gain rolloffs at both band edges. This is due to differences between the actual FETs and circuit elements and the models used in the design.

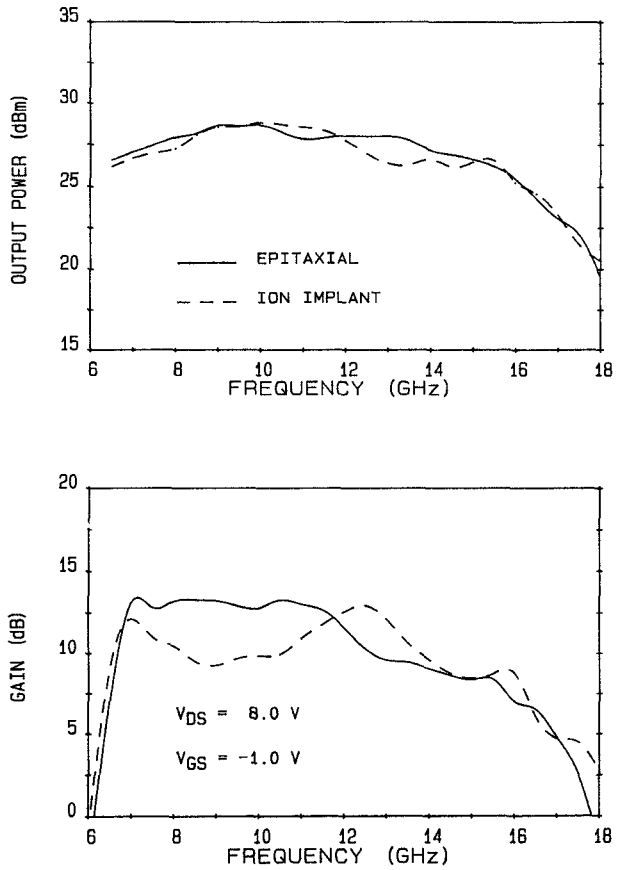

Figure 4. Measured amplifier performance (1 dB Gain Compression)

Measured power performance, at 1dB gain compression, of the epitaxial and ion implanted 900-1200 micron amplifiers averaged 27.4 dBm (550 mW) and 27.2 dBm (530 mW) across the 7.0 to 17.0 GHz band, which translates to 0.46 and 0.44 watts per millimeter of FET gate width. Under the same measurement conditions, average power-added efficiences were 18.7 and 18.9 percent, with average gains of 11.0 and 10.2 dB, respectively.

The 900-1200 micron amplifier was designed to be used in a balanced configuration. Figure 5

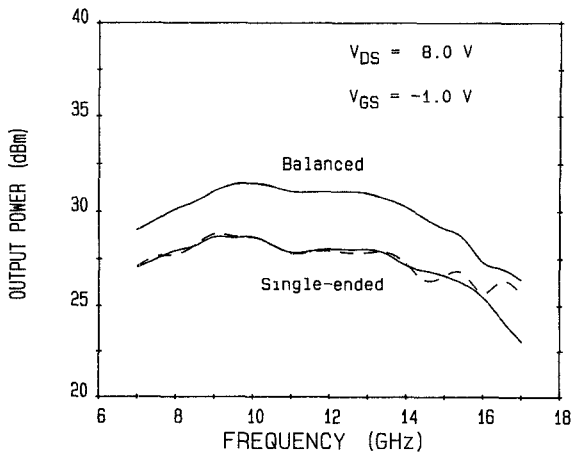

Figure 5. Balanced Amplifier Performance at 1 dB Gain Compression. The Chips Are From Two Different Slices

shows the combining efficiency achieved when balancing two chips from different slices. The chips were matched strictly from device I-V data, obtained prior to circuit assembly. The output power of each separate chip is shown, as well as the power obtained from the balanced pair. Across the 7.0-17.0 GHz frequency band, the balanced amplifier delivered an average of 30.1 dBm (1020 mW) at 1 dB gain compression. This represents an average combining efficiency of 2.5 dB, which compares well with results achieved using chips selected from the same slice.

CONCLUSION

First design iteration monolithic 900-1200 micron medium power amplifiers, from a number of epitaxial and ion implanted slices, have demonstrated excellent gain and output power performance across the 7.0-17.0 GHz frequency band. An average of 27.3 dBm (540 mW or 0.45 watts per millimeter of gate width), at 18.8 percent power-added efficiency, with an average gain of 10.6 dB, was achieved at 1 dB gain compression.